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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/823,276 | 03/29/2001 | Ryo Inoue | 10559-393001/P10258-ADI- | 7293 |

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FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER

O BRIEN, BARRY J

| | |
|----------|--------------|
| ART UNIT | PAPER NUMBER |
|----------|--------------|

2183

DATE MAILED: 08/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/823,276

Applicant(s)

INOUE ET AL.

Examiner

Barry J. O'Brien

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 06 May 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. Claims 1-21 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed on record in the file: Amendment A as received on 5/06/2004.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.
4. The applicant is requested to review the specification and update the status of all co-pending applications made mention of, replacing attorney docket numbers with current U.S. application or patent numbers when appropriate.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

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7. Claim 6 recites the limitation "the number of clock cycles it takes to flush a pipelined processor" on its second and third lines. It is unclear whether this "number of clock cycles" can be determined from any arbitrary pipelined processor, a pipelined processor that is associated with the future file of claim 1, or something else altogether. Please clarify the claim language to more clearly define the metes and bounds of the claimed invention.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-3, 6-8, 12, 15 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kishigami et al., U.S. Patent No. 5,155,817.

10. Regarding claim 1, Kishigami has taught a method comprising:

- a. Accessing a future file which is capable of being restored in a single clock cycle
(see Col. 8 lines 28-35 and Col.15 line 47 – Col.16 line 12).
- b. Restoring a future file over more than one clock cycle when a termination occurs
(see Col.18 lines 16-19, 42-45).

11. Regarding claim 2, Kishigami has taught the method of claim 1 as shown above, further comprising maintaining the future file in a pipelined processor (see Col.1 lines 5-12).

12. Regarding claim 3, Kishigami has taught the method of claim 1 as shown above, wherein restoring the future file comprises updating at least some speculative registers in the future file

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with architectural values (see Col.4 lines 42-46, Col.8 lines 28-34 and Col.18 lines 16-19, 42-45).

13. Regarding claims 7 and 15, taking claim 15 as exemplary, Kishigami has taught a system comprising:

- a. A static random access memory device (204 of Fig.9),
- b. A processor coupled to the static random access memory device, wherein the processor includes a first set of registers, a second set of registers, a pipeline and a control unit (see Col.8 lines 22-34 and Fig.1) capable of restoring the first registers with data contained in the second registers during a single clock cycle (see Col. 8 lines 28-35 and Col.15 line 47 – Col.16 line 12), but adapted to restore at least some of the registers in the first set of registers with values in at least some of the registers in the second set of registers over more than one clock cycle if a termination occurs in the pipeline (see Col.4 lines 42-46 and Col.18 lines 16-19, 42-45).

14. Claim 7 is nearly identical to claim 15. Claim 7 differs in its lack of a static random access memory device and a processor coupled to said memory device, but encompasses the same scope as claim 15. Therefore, claim 7 is rejected for the same reasons as claim 15.

15. Regarding claims 6, 12 and 19, taking claim 19 as exemplary, Kishigami has taught the method of claim 15 as shown above, wherein more than one clock cycle comprises the number of clock cycles it takes to flush the pipelined processor (see Col.18 lines 16-19, 42-45). Here, the “flush” of a pipeline requires that the pipeline be cleared of instructions and be restored to its previous known state so that non-speculative operation can continue. Because restoring to the

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previous state requires that the future file be restored to a known state, it is inherent that the number of clock cycles that it takes to restore the future file is the number of clock cycles it takes to flush the pipeline.

16. Claims 6 and 12 are nearly identical to claim 19. Claims 6 and 12 differ in their parent claims, but encompass the same scope as claim 19. Therefore, claims 6 and 12 are rejected for the same reasons as claim 19.

17. Regarding claim 8, Kishigami has taught the apparatus of claim 7 as shown above, wherein each register in the second set of registers is associated respectively with a register in the first set of registers (see Col.13 lines 45-52 and Col. 14 lines 25-44).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. Claims 4-5, 9-10 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishigami et al., U.S. Patent No. 5,155,817.

20. Regarding claims 4, 9 and 16, taking claim 16 as exemplary, Kishigami has taught the method of claim 15 as shown above, but has not explicitly taught wherein more than one clock cycle comprises two clock cycles.

21. However, Kishigami has taught that the amount of clock cycles required to restore the future file is directly dependent upon how many general-purpose architectural registers there are

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in the processor (see Col.18 lines 16-19, 42-45). Because the claim language has not limited the future file and/or architectural register file that correspond to the future file to a specific size, any size register file will satisfy the claim language. Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to modify the register file of Kishigami to include two general-purpose registers so that the amount of clock cycles to restore the future file becomes two cycles due to the direct dependence between the amount of general-purpose registers and clock cycles required to restore the future file corresponding to those registers.

22. Claims 4 and 9 are nearly identical to claim 16. Claims 4 and 9 differ in their parent claims, but encompass the same scope as claim 16. Therefore, claims 4 and 9 are rejected for the same reasons as claim 16.

23. Regarding claims 5, 10 and 17, taking claim 17 as exemplary, Kishigami has taught the method of claim 15 as shown above, but has not explicitly taught wherein more than one clock cycle comprises three clock cycles.

24. However, Kishigami has taught that the amount of clock cycles required to restore the future file is directly dependent upon how many general-purpose architectural registers there are in the processor (see Col.18 lines 16-19, 42-45). Because the claim language has not limited the future file and/or architectural register file that correspond to the future file to a specific size, any size register file will satisfy the claim language. Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to modify the register file of Kishigami to include three general-purpose registers so that the amount of clock cycles to restore the future file becomes three cycles due to the direct dependence between the amount of general-purpose registers and clock cycles required to restore the future file corresponding to those registers.

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25. Claims 5 and 10 are nearly identical to claim 17. Claims 5 and 10 differ in their parent claims, but encompass the same scope as claim 17. Therefore, claims 5 and 10 are rejected for the same reasons as claim 17.

26. Claims 11, 13, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kishigami et al., U.S. Patent No. 5,155,817, as applied to claims 7 and 15 above, respectively, and further in view of Ozer et al., *A Fast Interrupt Handling Scheme for VLIW Processors*.

27. Regarding claims 11 and 18, taking claim 18 as exemplary, Kishigami has taught the apparatus of claim 15 as shown above, but has not explicitly taught wherein the control unit is further adapted to flush the pipeline following termination of the instruction in the pipeline.

28. However, Ozer has taught when an exception occurs that the offending instruction is stopped and all pipelines are flushed prior to restoring the future file with values from the architectural register file (see Col.4 lines 16-20) so that the correct state of the processor is known during the interrupt even though out-of-order execution is taking place (see Col.2 lines 9-21), as well as to track which instructions cause the interrupts to occur (see Col.4 lines 20-29).

One of ordinary skill in the art would have recognized that it is desirable to microprocessor designers to operate a processor in a correct, known state so that the results of processing are correct and useful. Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to modify the processor of Kishigami to flush the pipeline following termination of an instruction in the pipeline so that the processor will operate in a known state and produce correct results.

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29. Claim 11 is nearly identical to claim 18. Claim 11 differs in its parent claim, but encompasses the same scope as claim 18. Therefore, claim 11 is rejected for the same reasons as claim 18.

30. Regarding claims 13 and 20, taking claim 20 as exemplary, Kishigami has taught the apparatus of claim 19 as shown above, but has not explicitly taught wherein the control unit is further adapted to restore at least one register in the first set of registers after the pipeline has been flushed.

31. However, Ozer has taught when an exception occurs that the offending instruction is stopped and all pipelines are flushed prior to restoring the future file with values from the architectural register file (see Col.4 lines 16-20) so that the correct state of the processor is known during the interrupt even though out-of-order execution is taking place (see Col.2 lines 9-21), as well as to track which instructions cause the interrupts to occur (see Col.4 lines 20-29). One of ordinary skill in the art would have recognized that it is desirable to microprocessor designers to operate a processor in a correct, known state so that the results of processing are correct and useful. Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to modify the processor of Kishigami to flush the pipeline following termination of an instruction in the pipeline so that the processor will operate in a known state and produce correct results.

32. Claim 13 is nearly identical to claim 20. Claim 13 differs in its parent claim, but encompasses the same scope as claim 20. Therefore, claim 13 is rejected for the same reasons as claim 20.

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33. Claims 14 and 21 rejected under 35 U.S.C. 103(a) as being unpatentable over Kishigami et al., U.S. Patent No. 5,155,817 as applied to claims 7 and 15 above, respectively, and further in view of Patterson et al., *Computer Organization and Design*.

34. Regarding claims 14 and 21, taking claim 21 as exemplary, Kishigami has taught the apparatus of claim 15 as shown above, but has not explicitly taught wherein the pipeline is an X-stage pipeline, the control unit adapted to restore the first set of registers with data contained in the second set of registers over X-N clock cycles or fewer, following a termination of an instruction in an Nth stage of the pipeline.

35. However, Patterson has taught a standard five-stage pipeline, which is a well-known and conventional configuration for a pipeline (see Patterson, p.450-453). Kishigami has taught the restoring of the processor state in order to process the unpredicted branch path in the event of a branch misprediction (see Kishigami, Col.18 lines 42-45) as well as having taught that the amount of clock cycles required to restore the future file is directly dependent upon how many general-purpose architectural registers there are in the processor (see Col.18 lines 16-19, 42-45). Because the claim language has not limited the future file and/or architectural register file that correspond to the future file to a specific size, any size register file will satisfy the claim language. Therefore, one of ordinary skill in the art at the time of the invention would have found it obvious to modify the register file of Kishigami to include two general-purpose registers so that the amount of clock cycles to restore the future file becomes two cycles due to the direct dependence between the amount of general-purpose registers and clock cycles required to restore the future file corresponding to those registers. Thus, because Patterson has taught the execution

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stage being the third stage of five (see Patterson, p.450), and five minus three is two (pipeline stages minus stage corresponding to the execution stage), the claim language has been satisfied.

36. Claim 14 is nearly identical to claim 21. Claim 14 differs in its parent claim, but encompasses the same scope as claim 21. Therefore, claim 14 is rejected for the same reasons as claim 21.

Response to Arguments

37. Applicant's arguments filed 5/06/2004 have been fully considered but they are not persuasive.

38. On p.10 lines 4-10 of the present amendment, the Applicant argues, in essence:

"Specifically, Kishigami refers to a "prototype" beginning at column 18, and that the prototype requires 16 cycles to empty the 16 general-purpose registers. It is apparent that 16 cycles are absolutely necessary to empty these registers, since Kishigami describes ... that this is undesirable, and that it can "deteriorate performance of the microprocessor"."

39. The Applicant is correct in noting that Kishigami describes the restoring of the future file over multiple cycles as undesirable. However, whether or not a limitation is desirable does not have any bearing on the claim limitation being allowable. Instead, whether or not the limitation has been taught by the prior art of record determines the allowability of claim limitations. The claimed limitation, specifically restoring a future file over multiple clock cycles, has been taught by Kishigami (see above paragraphs 10, 13 and 14), and thus remains rejected.

40. On p.10 lines 11-15 of the present amendment, the Applicant argues, in essence:

"Therefore, it is clear that the only time that Kishigami will restore the future file over more than one clock cycle, is when that is the only alternative. More specifically, whenever the future file is capable of being restored over a single clock cycle, it will be so restored."

41. The Examiner would like to point out that the Applicant is admitting that the prior art of reference, namely Kishigami, has taught all of the limitations of amended claims 1, 7 and 15, specifically that Kishigami has taught a future file capable of being restored over a single clock cycle, and the restoring of the future file over more than one clock cycle when a termination occurs.

42. On p.11 lines 1-13 of the present amendment, the Applicant argues, in essence:

"Kishigami does not teach or suggest a future file "which is capable of being restored in a single clock cycle" but yet is restored "over more than one clock cycle when the termination occurs" as defined in claim 1. Rather, Kishigami teaches that a special prototype which requires multiple clock cycles to restore the future file is restored over those multiple clock cycles, but only because that is absolutely necessary. Kishigami describes the general undesirability of restoring a future file over multiple clock cycles. This demonstrates the unobviousness of the present system which specifically teaches restoring a future file over more than one clock cycle even though that future file is capable of being restored in a single clock cycle."

43. However, Kishigami has taught a future file which is capable of being restored in a single clock cycle but is restored over more than one clock cycle when a termination occurs (see above

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paragraphs 10, 13 and 14). In fact, the Applicant has admitted that Kishigami has taught such a future file (see p.10 lines 11-15 of the present amendment filed on 5/06/2004).

44. Furthermore, the Applicant is correct in noting that Kishigami describes the restoring of the future file over multiple cycles as undesirable. However, whether or not a limitation is desirable does not have any bearing on the claim limitation being allowable. Instead, whether or not the limitation has been taught by the prior art of record determines the allowability of claim limitations. The claimed limitation, specifically restoring a future file over multiple clock cycles, has been taught by Kishigami (see above paragraphs 10, 13 and 14), and thus remains rejected.

45. On p.11 lines 14-20 of the present amendment, the Applicant argues, in essence:

"Claim 1 defines the subject matter, and specifically accessing the future file which is capable of being restored in the single clock cycle, and restoring that future file over more than one clock cycle when the termination occurs. Therefore, claim 1 defines subject matter which is novel over Kishigami, and which goes against the express teaching in Kishigami."

46. However, Kishigami has taught "accessing the future file which is capable of being restored in the single clock cycle, and restoring that future file over more than one clock cycle when the termination occurs" (see above paragraphs 10, 13 and 14). In fact, the Applicant has admitted that Kishigami has taught such a future file (see p.10 lines 11-15 of the present amendment filed on 5/06/2004). Furthermore, the limitations of Claim 1, which are taught by Kishigami, inherently cannot be considered to be going "against the express teaching" of Kishigami when the limitations are, in fact, taught by the reference.

Conclusion

47. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

48. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Barry J. O'Brien whose telephone number is (703) 305-5864. The examiner can normally be reached on Mon.-Fri. 6:30am-4:00pm.

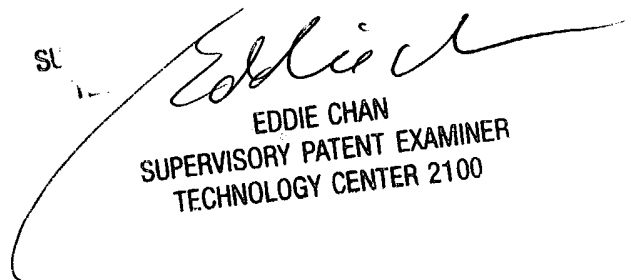
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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50. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Barry J. O'Brien
Examiner
Art Unit 2183

BJO
8/4/2004

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